

Rectangular De-Interleaver

Features

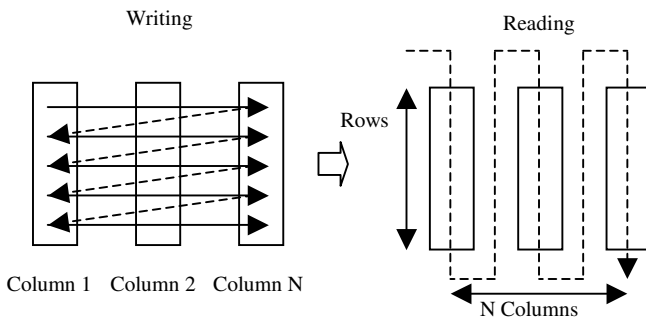
- High speed Rectangular de-interleaver
- Fully pipelined
- Available for all vendors
- Easy to use interface signals
- Configurable data input size
- Support many standards as DVB or CDMA2000
- Generic configurable number of columns
- Dynamic configurable number of rows
- Selection of logic or RAM for implementation

Application

The De-interleaver is compliant with many communication systems as DVB or CDMA2000. The dynamic configuration permits to perform many applications.

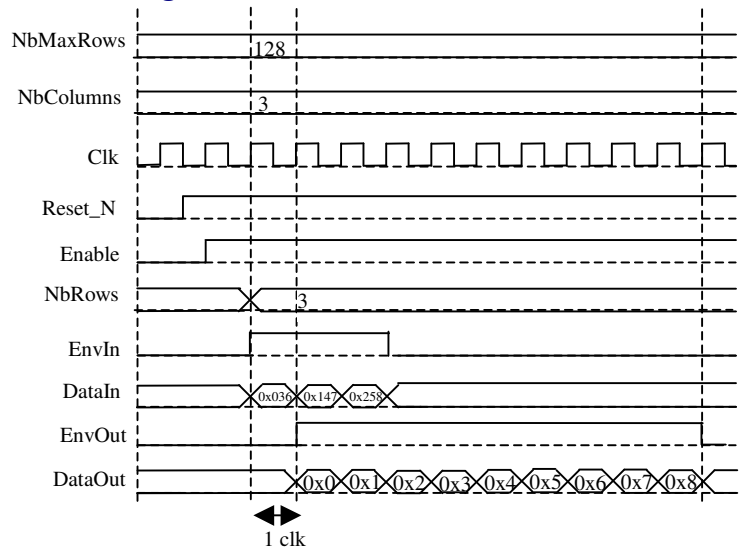
Functional description

The De-Interleaver core unscrambles data with the rectangular method. Data are rearranged as shown below :



De-interleaving is the reverse operation of Interleaving.

Timing



I/O

Signal	Direction	Width	Function
LengthData	Generic Integer		Data size
NbColumns	Generic Integer		Number of columns
NbMaxRows	Generic Integer		Maximum number of columns
Mode	Generic Integer		Implementation mode (RAM =1, Logic =0)
Clk	IN	1 bit	Input clock
Reset_n	IN	1 bit	Reset (active Low)
Enable	IN	1 bit	Enable
EnvIn	IN	1 bit	Input envelop
NbRows	IN	NbMaxRows	Number of rows in the interleaver
DataIn	IN	LengthData	Input Data
EnvOut	OUT	1 bit	Output envelop
DataOut	OUT	NbColumns* LengthData	Interleaved data

Performance characteristics

The Rectangular De-Interleaver occupies 254 slices on Xilinx Virtex 2 and the synthesis frequency is 234MHz, for a 9 bits data input, 4 columns, 128 rows maximum for logic implementation scheme.