

## Features

- High speed DVB-S2 mapper
- Compliant with DVB-S2 standard [1]
- Fully pipelined
- Available for all vendors
- Easy to use interface signals
- Configurable output length

## Application

The DVB-S2 mapper core is compliant with the DVB-S2 standard [1].

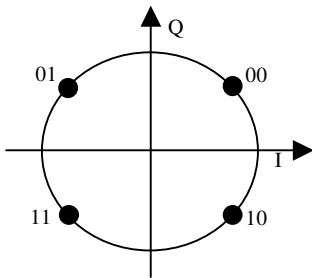
## Functional description

The DVB-S2 mapper core generates symbols coded on 2's complements. The output values are quantified between [-2;2] (due to the APSK modulations), rounded to the closest integer.

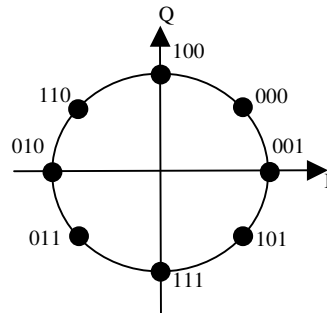
QPSK maps 2 bits (the 2 LSB of LabelIn), 8PSK 3 bits (3 LSB), 16-APSK 4 bits (4LSB) and 32-APSK 5 bits.

The module is fully pipelined which enables high rates. The mapping for each modulation is shown below :

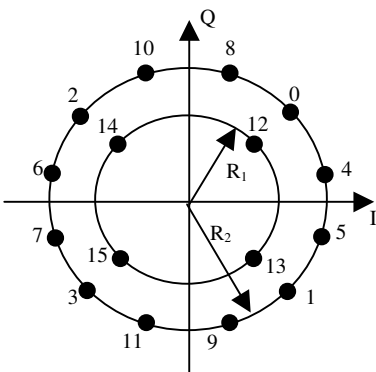
QPSK Mode:



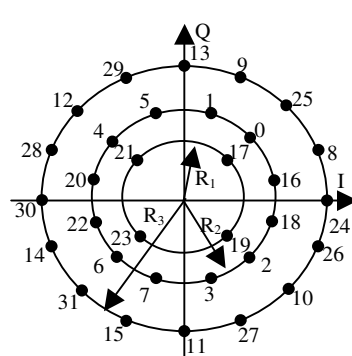
8PSK Mode:



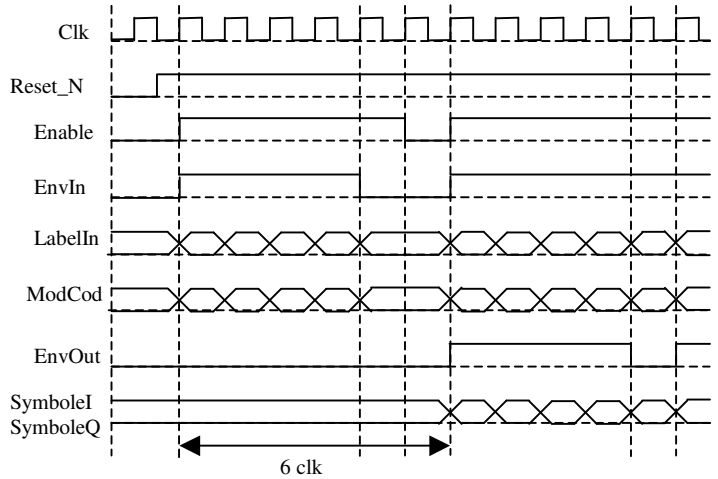
16APSK Mode:



32APSK Mode:



## Timing



## I/O

Signal	Direction	Width	Function
LengthOut	Generic Integer	14	Symbol size
Clk	IN	1 bit	Input clock
Reset_n	IN	1 bit	Reset (active Low)
Enable	IN	1 bit	Enable
Envin	IN	1 bit	Input envelop
Modcod	IN	5 bits	Modulation and rate selection
LabelIn	IN	5 bits	Input bits
SymboleI	OUT	LengthOut	Symbol I
SymboleQ	OUT	LengthOut	Symbol Q
EnvOut	OUT	1 bit	Output envelop

Mode	ModCod	Mode	ModCod	Mode	ModCod	Mode	ModCod
QPSK	1	QPSK	9	8PSK	17	32APSK	25
QPSK	2	QPSK	10	16APSK	18	32APSK	26
QPSK	3	QPSK	11	16APSK	19	32APSK	27
QPSK	4	8PSK	12	16APSK	20	32APSK	28
QPSK	5	8PSK	13	16APSK	21	Reserved	29
QPSK	6	8PSK	14	16APSK	22	Reserved	30
QPSK	7	8PSK	15	16APSK	23	Reserved	31
QPSK	8	8PSK	16	32APSK	24	plframe	0

## Performance characteristics

The DVB-S2 mapper occupies 239 slices on Xilinx Virtex 2, and the synthesis frequency is 233MHz.

## Reference

[1] ETSI EN 302 307 V1.1.1 (2004-06)