

Features

- High speed LDPC Decoder
- Compliant with DVB-S2 standard [1]
- Short (16200 bits) and Normal (64800 bits) frame compliant
- All rates available (1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10)
- Available for all vendors
- Easy to use interface signals

Application

The DVB-S2 LDPC Decoder core is compliant with the DVB-S2 standard [1].

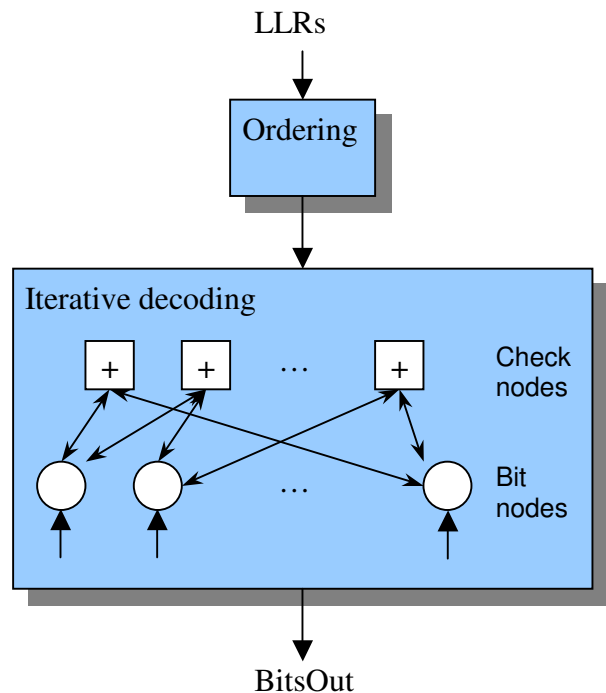
I/O

Main IOs are described in the table below :

Signal	Direction	Width	Function
Clk_data	IN	1 bit	LLRs Clock
Reset_n	IN	1 bit	Reset (active Low)
ModcodIn	IN	7 bits	MODCOD and Type of the coming data
LLR0 to LLR4	IN	5x 6 bits	Input LLRs
Nbliteration sMax	IN	6 bits	Maximum of iterations numbers
EnvIn	IN	1 bit	LLRs envelop
EnvOut	OUT	1 bit	Output envelop
DataOut	OUT	9 bits	Output Data
Decoding	OUT	1 bit	Frame is decoding
Nblte	OUT	6 bits	Number of decoding iterations
ModcodOut	OUT	7 bits	MODCOD and Type of the output data

Functional description

The DVB-S2 LDPC Decoder orders LLRs on the fly and start decoding once the full frame is received. Iterative decoding is performed and stops when the decoder converges to a code word or reached the maximum iterations number defined. The maximum iteration number is selectable from 1 to 63 iterations.



Performance characteristics

The DVB-S2 LDPC is available and optimized for Xilinx Virtex 2Pro, Virtex 4 and Virtex 5.

Reference

[1] ETSI EN 302 307 V1.1.1 (2004-06)

Timing

