

## Features

- High speed BCH Decoder
- Compliant with DVB-S2 standard [1]
- Short (16200 bits) and Normal (64800 bits) frame compliant
- All rates available (1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10)
- Fully pipelined
- Available for all vendors
- Easy to use interface signals

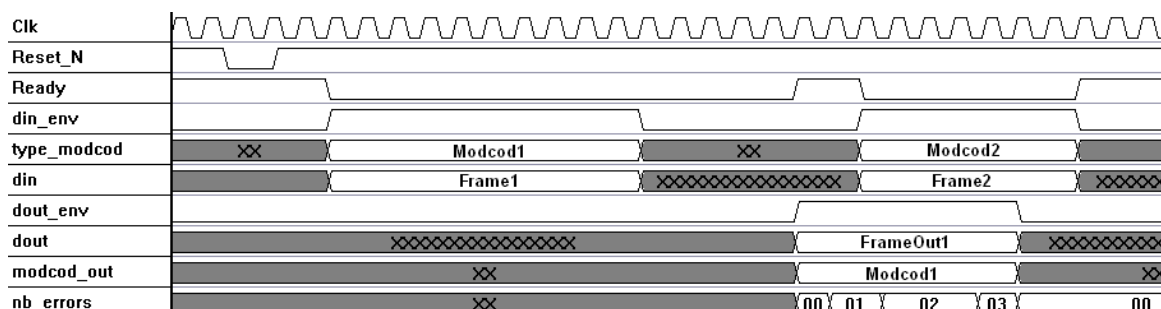
## Application

The DVB-S2 BCH Decoder core is compliant with the DVB-S2 standard [1].

## I/O

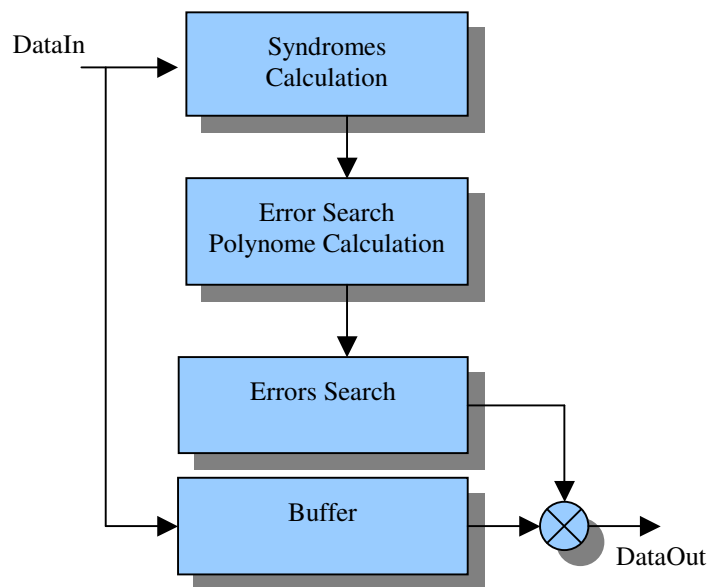
Signal	Direction	Width	Function
Clk	IN	1 bit	Input clock
Reset_n	IN	1 bit	Reset (active Low)
type_modcod	IN	7 bits	MODCOD and Type of the coming data
din	IN	1 bit	Input Data
din_env	IN	1 bit	Input envelop
dout_env	OUT	1 bit	Output envelop
dout	OUT	1 bit	Output Data (reverse order)
ready	OUT	1 bit	Module ready
nb_errors	OUT	4 bit	Number of corrected errors
modcod_out	OUT	7 bits	MODCOD and Type of the output data

## Timing



## Functional description

The DVB-S2 BCH Decoder core is able to correct up to 8, 10 or 12 errors at any place in the frame, depending on the standard. The decoder is performing Syndromes Calculation first. Then, it computes the Errors Search Polynome, and finally locates and corrects the errors.



## Performance characteristics

The DVB-S2 BCH Decoder occupies 5800 slices and 5 RAM on Xilinx Virtex 2 Pro, and the synthesis frequency is 140MHz.

## Reference

[1] ETSI EN 302 307 V1.1.1 (2004-06)